AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Original) A frequency synthesizer comprising:

a ring oscillator circuit, which receives a pair of input signals and is operable to generate a pair of oscillating signals;

duty buffers, which receive the pair of oscillating signals, respectively and are operable to generate output signals with predetermined duty cycles, respectively;

half adders, which receive the predetermined duty cycle signals from the duty buffers and generate a first output signal as a result of an Exclusive-OR (XOR) operation on the output signals of the duty buffers and an output signal as a result of an AND operation on the predetermined duty cycle signals; and

a switch, which selects one of the oscillating signals of the ring oscillator circuit, the XOR result and the AND result, according to a switch-control signal.

2. (Original) The frequency synthesizer of claim 1, wherein the ring oscillator circuit includes an even number of ring oscillators, receives the pair of input signals at a pair of input terminals and feeds back the pair of oscillating signals to the pair of input terminals.

3. (Original) The frequency synthesizer of claim 2, wherein each of the ring oscillators comprises:

first and second PMOS transistors having sources connected to a supply voltage and whose gates are connected to a first bias signal;

a third PMOS transistor having a source connected to a drain of the first PMOS transistor and a gate connected to a first one of the pair of input signals;

a first NMOS transistor having a drain connected at a first node to a drain of the third PMOS transistor and a gate connected to receive the first one of the pair of input signals;

a fourth PMOS transistor having a source is connected to a drain of the second PMOS transistor and a gate connected to receive a second one of the pair of input signals;

a second NMOS transistor having a drain connected at a second node to a drain of the fourth PMOS transistor and a gate connected to receive the second one of the pair of input signals;

a third NMOS transistor having a gate connected to receive a control signal, a drain connected to sources of the first and second NMOS transistors, and a drain connected to ground voltage;

a fifth PMOS transistor having a source and a drain respectively connected to source and drain of the third PMOS transistor, a gate of the fifth PMOS transistor being connected to the source thereof;

a sixth PMOS transistor having a source and a drain respectively connected to the gate and drain of the fourth PMOS transistor, a gate of the sixth PMOS transistor being connected to the source thereof;

a fourth NMOS transistor having a drain connected to the drain of the fifth PMOS transistor and a gate connected to the drain of the sixth PMOS transistor;

a fifth NMOS transistor having a drain connected to the drain of the sixth PMOS transistor and a gate connected to the drain of the fifth PMOS transistor; and

a sixth NMOS transistor having a gate connected to receive a second bias signal, a drain sources of the fourth and fifth NMOS transistors, and a gate connected to the ground voltage,

wherein signals on the first and second nodes represent the pair of oscillating signals.

4. (Original) The frequency synthesizer of claim 1, wherein the duty cycles of output signals of the duty buffers are about 50%.

5. (Original) The frequency synthesizer of claim 1, wherein each of the duty buffers comprises:

a first PMOS transistor having a source connected to the supply voltage and a gate connected to receive a first one of the input signals;

a second PMOS transistor having a source connected to the supply voltage and a gate

connected to receive a second one of the input signals;

first and second NMOS transistors having drains and gates connected a first and second nodes to the drains of the first and second PMOS transistors, respectively;

a third PMOS transistor having a source connected to the supply voltage and a gate connected to the first node;

a fourth PMOS transistor having a source connected to the supply voltage and a gate connected to the second node;

third and fourth NMOS transistors having drains are connected to the drains of the third and fourth PMOS transistors, respectively, and sources connected to a ground voltage, and gates connected to the drain of the third NMOS transistor; and

serially-connected inverters, an input to a first one of the inverters being connected to the drains of the fourth PMOS transistor and the fourth NMOS transistor.

6. (Original) The frequency synthesizer of claim 1, further comprising:

a decoder to decode a frequency selection signal and produce the switch-control signal.

7. (Original) A frequency synthesizer comprising:

a ring oscillator circuit, which receives a pair of input signals and, in response to a control signal, is operable to generate a pair of first oscillating signals, a pair of second oscillating signals, and a pair of third oscillating signals that are delayed with respect to each other;

first and second duty buffer circuits, which receive the pair of first oscillating signals and the pair of second oscillating signals and in response generate first and second duty signals, respectively;

half adder means for receiving output signals of the duty buffer means and for responsively generating a first output signal according to an Exclusive-OR operation upon the first and second duty signals and a second output signal according to an AND operation upon the first and second duty signals; and

switch means for selecting one of the third pair of oscillating signals, the first output signal and the second output signal.

8. (Original) The frequency synthesizer of claim 7, the ring oscillator means is further operable for scaling frequencies of the first pair of oscillating signals, the second pair of oscillating signals, and the third pair of oscillating signals to be proportional with the voltage level of the control signal.

9. (Original) The frequency synthesizer of claim 7, wherein the ring oscillator circuit comprises:

first ring oscillator means for receiving the pair of input signals and for generating the pair of first oscillating signals;

second ring oscillator means for receiving the pair of first oscillating signals;

third ring oscillator means for receiving output signals of the second ring oscillator and for generating the pair of second oscillating signals; and

fourth ring oscillator means for receiving the pair of second oscillating signals, for generating the pair of third oscillating signals, and for feeding back the pair of third oscillating signals to input terminals of the first ring oscillator means.

10. (Currently Amended) The frequency synthesizer of claim 7, wherein the ring oscillator circuit comprises:

first and second PMOS transistors having sources connected to a supply voltage and whose gates are connected to a first bias signal;

a third PMOS transistor having a source connected to a drain of the first PMOS transistor and a gate connected to a first one of the pair of input signals;

a first NMOS transistor having a drain connected at a first node to a drain of the third PMOS transistor and a gate connected to receive the first one of the pair of input signals;

a fourth PMOS transistor having a source ~~is~~ connected to a drain of the second PMOS transistor and a gate connected to receive a second one of the pair of input signals;

a second NMOS transistor having a drain connected at a second node to a drain of the fourth PMOS transistor and a gate connected to receive the second one of the pair of input signals;

a third NMOS transistor having a gate connected to receive a control signal, a drain connected to sources of the first and second NMOS transistors, and a drain connected to ground voltage;

a fifth PMOS transistor having a source and a drain respectively connected to source and drain of the third PMOS transistor, a gate of the fifth PMOS transistor being connected to the source thereof;

a sixth PMOS transistor having a source and a drain respectively connected to the gate and drain of the fourth PMOS transistor, a gate of the sixth PMOS transistor being connected to the source thereof;

a fourth NMOS transistor having a drain connected to the drain of the fifth PMOS transistor and a gate connected to the drain of the sixth PMOS transistor;

a fifth NMOS transistor having a drain connected to the drain of the sixth PMOS transistor and a gate connected to the drain of the fifth PMOS transistor; and

a sixth NMOS transistor having a gate connected to receive a second bias signal, a drain sources of the fourth and fifth NMOS transistors, and a gate connected to the ground voltage,

wherein signals on the first and second nodes represent one of the pairs of oscillating signals.

11. (Original) The frequency synthesizer of claim 7, wherein each of the duty buffers comprises:

a first PMOS transistor having a source connected to the supply voltage and a gate connected to receive a first one of the input signals;

a second PMOS transistor having a source connected to the supply voltage and a gate connected to receive a second one of the input signals;

first and second NMOS transistors having drains and gates connected a first and second nodes to the drains of the first and second PMOS transistors, respectively;

a third PMOS transistor having a source connected to the supply voltage and a gate connected to the first node;

a fourth PMOS transistor having a source connected to the supply voltage and a gate connected to the second node;

third and fourth NMOS transistors having drains are connected to the drains of the third and fourth PMOS transistors, respectively, and sources connected to a ground voltage, and gates connected to the drain of the third NMOS transistor; and

serially-connected inverters, an input to a first one of the inverters being connected to the drains of the fourth PMOS transistor and the fourth NMOS transistor.

12. (Original) The frequency synthesizer of claim 7, wherein the switch means is further operable for decoding a frequency selection signal and for making the selection based upon the frequency selection signal.

13. (Original) A frequency synthesizing method comprising:

receiving a pair of input signals;

generating response to a control signal, a pair of first oscillating signals, a pair of second oscillating signals, and a pair of third oscillating signals that are delayed with respect to each other;

generating first and second duty signals based upon the pair of first oscillating signals and the pair of second oscillating signals, respectively;

generating a first output signal as a result of an Exclusive-OR operation upon the first and second duty signals;

generating a second output signal as a result of an AND operation upon the first and second duty signals; and

selecting one of the third pair of oscillating signals, the first output signal and the second output signal.

14. (Original) The frequency synthesizing method of claim 13, wherein the generation of pairs of oscillating signals includes:

scaling the ring frequencies of the first pair of oscillating signals, the second pair of oscillating signals, and the third pair of oscillating signals to be proportional with the voltage level of the control signal.

14. (Original) The frequency synthesizing method of claim 13, wherein the duty cycles of the first and second duty signals are about 50%.

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